

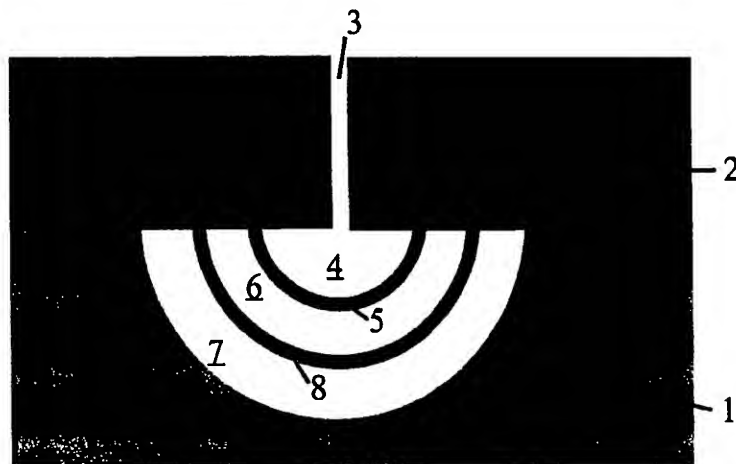
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(54) Title: **METHOD FOR ELECTROCHEMICALLY ETCHING A P-TYPE SEMICONDUCTING MATERIAL, AND A SUBSTRATE OF AT LEAST PARTLY POROUS SEMICONDUCTING MATERIAL**



(57) Abstract

The invention relates to a method of electrochemically etching a p-type semiconductor material, characterized by the following steps: a) the application of mask material on a substrate of the p-type semiconductor material; b) the local removal of the mask material; and c) placing the substrate with the mask into a corrosive electrolytic solution while simultaneously applying a current density through the substrate; wherein the current density during step c) is adjusted alternatingly to a high value causing the semiconductor material to be completely etched away, and a low value corroding the semiconductor material such as to become porous.

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Method for electrochemically etching a p-type semi-conducting material and a substrate of at least partly porous semiconducting material

The invention relates to a method of electrochemically etching a p-type semiconductor material.

Such a method is disclosed in the article "Porous Silicon: Microstructure, Optical Properties and Application to Light Emitting Diodes" by Y. Kanemitsu, T. Matsumoto, T. Futagi and H. Mimura, published in "Porous Silicon", World Scientific Singapore (1994), pages 363-367. This publication describes the fabrication of free-standing porous silicon in an electrochemical cell. To this end a p-type silicon substrate is exposed to a potential difference which is applied to the substrate, while the substrate is introduced into a solution of hydrogen fluoride (HF). During etching, a constant current density is applied for a predetermined period of time, after which the current density is abruptly increased to etch off the porous silicon from the substrate. The porous silicon is subsequently rinsed.

In accordance with the invention a method is now proposed for electrochemically etching a p-type semiconductor material, comprising the following steps:

- a) the application of mask material on a substrate of the p-type semiconductor material;
- b) the local removal of the mask material; and
- c) placing the substrate with the mask into a corrosive electrolytic solution while simultaneously applying a current density through the substrate, the current density during step c being adjusted alternately to a high value causing the semiconductor material to be completely etched away, and a low value corroding the semiconductor material such as to become porous.

In this manner a totally new product is provided which is equipped with specific microstructures, as will be explained below.

The invention is therefore also embodied in a substrate of at least partly porous semiconductor material coated with mask material. According to the invention the mask material is characterized in that on the substrate
5 side, the mask material has at least a structure of porous semiconductor material defining a channel that is free of semiconductor material. Such a substrate can be fabricated by the method according to the invention.

As already mentioned, a substrate of this kind is
10 completely novel. There are various useful prospective applications for such a substrate because the channel is at least partly defined by the porous semiconductor material. Such a substrate may be used, for instance, as a tubular sieve, as μ -battery, as carrier material for a
15 catalyst, as ion exchanger, as dosing system, but other applications are also conceivable. The above description must therefore be understood as enumeration and not as limitation.

The method according to the invention may be real-
20 ized satisfactorily by an embodiment in which the high current density value is above a critical current density value, and the low value is below the critical current density value, wherein - at least in the case of silicon - the critical current density value is determined at
25 approximately half the height of the first peak in the current voltage curve of the substrate when the same is placed in the electrolytic solution. For semiconductors other than silicon, this may be performed in a similar manner.

30 It has been proven to be useful to determine the critical current density value depending on the concentration in the electrolytic solution, such that at a higher concentration a higher critical current density value is chosen.

35 Conceivably the method in step c commences by etching away the substrate by applying a high current density value followed by the alternating application of a low current density value and then a high current density value. However, preferably the current density is first

set at the low value and after a predetermined first period of time is set at the high value which is maintained for a predetermined period of time, after which etching is discontinued. In this way the porous wall of the channel to be realized is applied directly to the mask material, which provides a more stable structure. If complete etching of the substrate is commenced in step c, it is also possible to use another technique such as plasma etching or KOH etching instead of the above-described method of electrochemical etching at high current density.

In a further aspect of the invention it is desirable to set the low current density to a value that depends on the desired pore size, such that for a large pore, the low current density value is adjusted to a high setting.

According to an interesting embodiment, the current density is first set at the high value, and after a predetermined first period of time it is set at a low value which is maintained for a predetermined second period of time, after which the current density is set at the high value and after a predetermined third period of time, etching is discontinued.

This method allows a porous structure to be formed at some distance removed from the original substrate surface.

The invention also relates to a method which is characterized in that preceding step a)

i) a groove structure is made into the substrate;
ii) the groove structure is filled with a material which under the conditions described in step c) is substantially unaffected and which, in comparison with the substrate material, conducts current poorly or not at all; and

iii) the substrate is coated with a mask material in step a) a material that under the conditions described in step c) is substantially unaffected and which, in comparison with the substrate material, conducts current poorly or not at all.

Such a method allows the fabrication of smooth structures. In addition, such structures are connected with a material located in the interior of the substrate body, rendering the structures less fragile. The groove
5 structure may conveniently be a groove structure extending all round, defining a substrate column.

The invention also relates to a substrate with a substantially partly porous semiconductor material that can be fabricated by the method described above. Said
10 substrate is characterized in that the substrate has at least one structure of porous semiconductor material comprising two substantially planar-parallel surfaces and which over its circumference is defined by and connected with a wall formed from wall material whose composition
15 differs from that of the porous semiconductor material, with the planar-parallel surfaces being over at least a portion of their surface free from substrate and from the wall material.

In general, the product obtained by the method is
20 pre-eminently suited for applications in micromachining, with the result that miniaturization of products in, for example, the above-mentioned fields of application is in the offing. The reduction in cost that can be realized thanks to the invention, may motivate a series of new
25 products which, because of the low cost, could also be single-use products.

The invention will now be explained in more detail with reference to the drawings, which

in Figs. 1 and 2 show the product according to the
30 invention in two alternative embodiments; and

in Fig. 3 illustrate a method for the manufacture of a product according to the invention.

In Figs. 1, 2 and 3 reference number 1 indicates a substrate of p-type semiconductor material, for example p-
35 type silicon. However, it is also possible to use other porous electrochemical etching material for this purpose. This p-type silicon is coated with mask material 2. Into the mask material 2 a hole is made locally to allow etching of the substrate 1. In a manner that is known, the

substrate 1 is for this purpose provided with a potential difference by applying a positive voltage to the side of the substrate 1 that faces away from the mask material 2. The negative potential is applied to the side of the mask material 2. As mask material 2 it is possible to use, for example, n-type silicon or silicon nitride. During the etching operation the current density through the substrate is set such as to alternate between a high value whereby the semiconductor material is etched away completely, and a low value whereby the semiconductor material is etched such as to become porous. When commencing the process for completely etching away that is to say when a high value of current density is being applied, the structure shown in Fig. 1 will ensue. Under the mask material, this structure is provided with a channel 4 which is partly defined by an arched structure 5 of porous semiconductor material. Due to alternation of said current densities the channels 6 and 7 are realized, which are still separated from one another by a further arched structure 8 of porous semiconductor material.

The low value and the high value of the current density are determined in relation to a critical current density such that the high value of the current density lies above the critical value of current density, and the low value lies below the critical value of current density. The critical current density value is set at approximately half the height of the first peak in the current density curve of the substrate when the same is placed into the electrolytic solution. Said critical current density value is then preferably determined subject to the concentration of the electrolytic solution such that at a higher concentration of the electrolyte, the critical current density value will also be chosen to be higher. In the porous-etching step, where the current density is set at a low value, it is possible to influence the pore size by a suitable selection of the low value of current density. This is done such that for a large pore the low current density value is adjusted to a high setting.

Fig. 2 shows the product to be obtained according to the invention when the procedure commences in step c with the application of a low current density value. In this way, first a portion of porous semiconductor material 9 is formed. Subsequent etching at high current density will form a channel 10 deeper down, which in turn may be defined by an arched structure 11 of porous semiconductor material that was formed by etching at a low current density following the preceding complete etching performed to form channel 10. Finally, the porous etching step may be succeeded by another complete-etching step during which channel 12 is formed. The said arched structures are attached to the mask material 2. Suitable selection of the application periods of low and high current densities respectively, allows the dimensions of the channels and the arched structures of porous semiconductor material defining said channels, to be adjusted. It should be noted that the porous silicon of the arched structures may optionally be provided with a coating, or be converted into silicon oxide, silicon nitride, silicon carbide, or metal silicides in manners that are known to the person skilled in the art, and which require no further explanation. By suitably selecting the process conditions under which porous etching takes place, the pore sizes in the porous silicon may be adjusted to a diameter of a few nanometres to several hundred of nanometre.

Example 1

A wafer of semiconductor material for etching or porous etching respectively, is introduced into an electrolyte of hydrogen fluoride. The strength of the porous structures depends, among other things, on the degree of doping of the silicon substrate. A suitable doping value for the silicon is, for example, approximately 10^{19} atoms/cm₃ (specific resistance 0.01 - 0.018 Ω cm). The critical current density value i_{crit} is then determined at approximately half the height of the first peak in the current voltage curve of the substrate after its introduction into the electrolyte. If the above-mentioned hydrogen

fluoride is used as the electrolyte, the resulting values are as shown in the table below.

5	[HF] (%)	i_{crit} (mA/cm ²)
	10	75
	5	22
	1	3

10

Example 2

Fig. 3 schematically shows how a substrate can be provided with a smooth structure of porous semiconductor material. A slice of silicon 1 is first provided with a groove structure 13 (Fig. 3a); in the present example it is a groove extending all round so that it defines a substrate column. The groove structure 13 is shaped as a square. The groove is 5 μ m wide and 60 μ m deep. By means of LDCVD, the silicon substrate is then coated with a layer of silicon nitride 14, thereby filling the groove structure 13 with silicon nitride (Fig. 3b). Subsequently, using the RIE process which is well-known in the field, an opening 3 is etched into the silicon nitride layer 14. Then silicon is removed at high current density (Fig. 3d), and porous silicon is formed at low current density (Fig. 3e). The result, after the subsequent removal of silicon by using a high current density, is a smooth structure 5 formed of porous silicon (Fig. 3f).

To the person skilled in the art it will be obvious that a variety of embodiments are possible using this method, which are all deemed to be within the scope of the invention. The current density may, for instance, be gradually increased or decreased during the formation of the porous structure 5. This results in an asymmetrical pore distribution over the porous structure 5. By means of, for example, a vacuum, the space 15 under the structure 5 can

be filled with a liquid comprising, for example, a protein or a drug. Furthermore, in the space 15 the substrate 1 may be provided with an electrode, and on the external surface, for example, around the porous structure 5, with
5 a counter electrode. By applying a voltage to the two electrodes, controlled release of the protein or the drug may be effectuated.

CLAIMS

1. A method of electrochemically etching a p-type semiconductor material, characterized by the following steps:

- a) the application of mask material on a substrate
5 of the p-type semiconductor material;
- b) the local removal of the mask material; and
- c) placing the substrate with the mask into a corrosive electrolytic solution while simultaneously applying a current density through the substrate;

10 wherein the current density during step c is adjusted alternately to a high value causing the semiconductor material to be completely etched away, and a low value corroding the semiconductor material such as to become porous.

15 2. A method according to claim 1, characterized in that the high current density value is above a critical current density value, and the low value is below the critical current density value, wherein the critical current density value is determined at approximately half the
20 height of the first peak in the current voltage curve of the substrate when the same is placed in the electrolytic solution.

3. A method according to claim 2, characterized in that the critical current density value depends on the
25 concentration in the electrolytic solution, such that at a higher concentration a higher critical current density value is chosen.

4. A method according to one of the claims 1-3, characterized in that the current density is first set at
30 the low value and after a predetermined first period of time is set at the high value which is maintained for a predetermined period of time, after which etching is discontinued.

5. A method according to one of the claims 1-3,
35 characterized in that the current density is first set at the high value, and after a predetermined first period of

time it is set at a low value which is maintained for a predetermined second period of time, after which the current density is set at the high value and after a predetermined third period of time, etching is discontinued.

5 6. A method according to one of the claims 1-5, characterized in that the low current density is set to a value that depends on the desired pore size, such that for a large pore, the low current density value is adjusted to a high setting.

10 7. A method according to claim 1 and one of the claims 5 or 6, characterized in that preceding step a)
 i) a groove structure is made into the substrate;
 ii) the groove structure is filled with a material which under the conditions described in step c) is substantially unaffected and which, in comparison with the
15 substrate material, conducts current poorly or not at all.

 8. A substrate of at least partly porous semiconductor material coated with mask material, characterized in that on the substrate side, the mask material has at
20 least a structure of porous semiconductor material defining a channel that is free of semiconductor material.

 9. A substrate with at least partly porous semiconductor material, characterized in that the substrate has at least one structure of porous semiconductor material
25 comprising two substantially planar-parallel surfaces and which over its circumference is defined by and connected with a wall formed from wall material whose composition differs from that of the porous semiconductor material, with the planar-parallel surfaces being over at least a
30 portion of their surface free from substrate and from the wall material.

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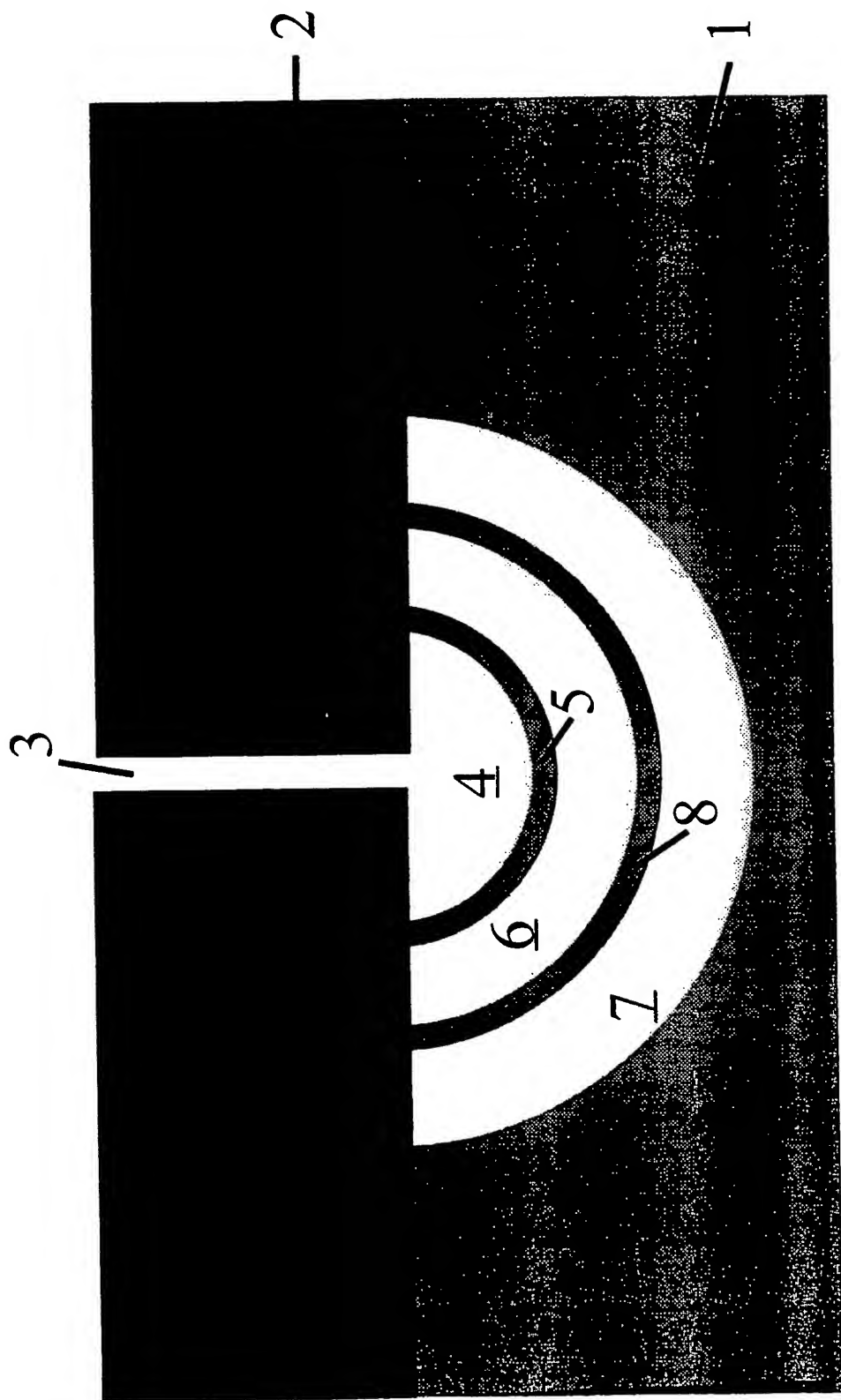


FIG. 1

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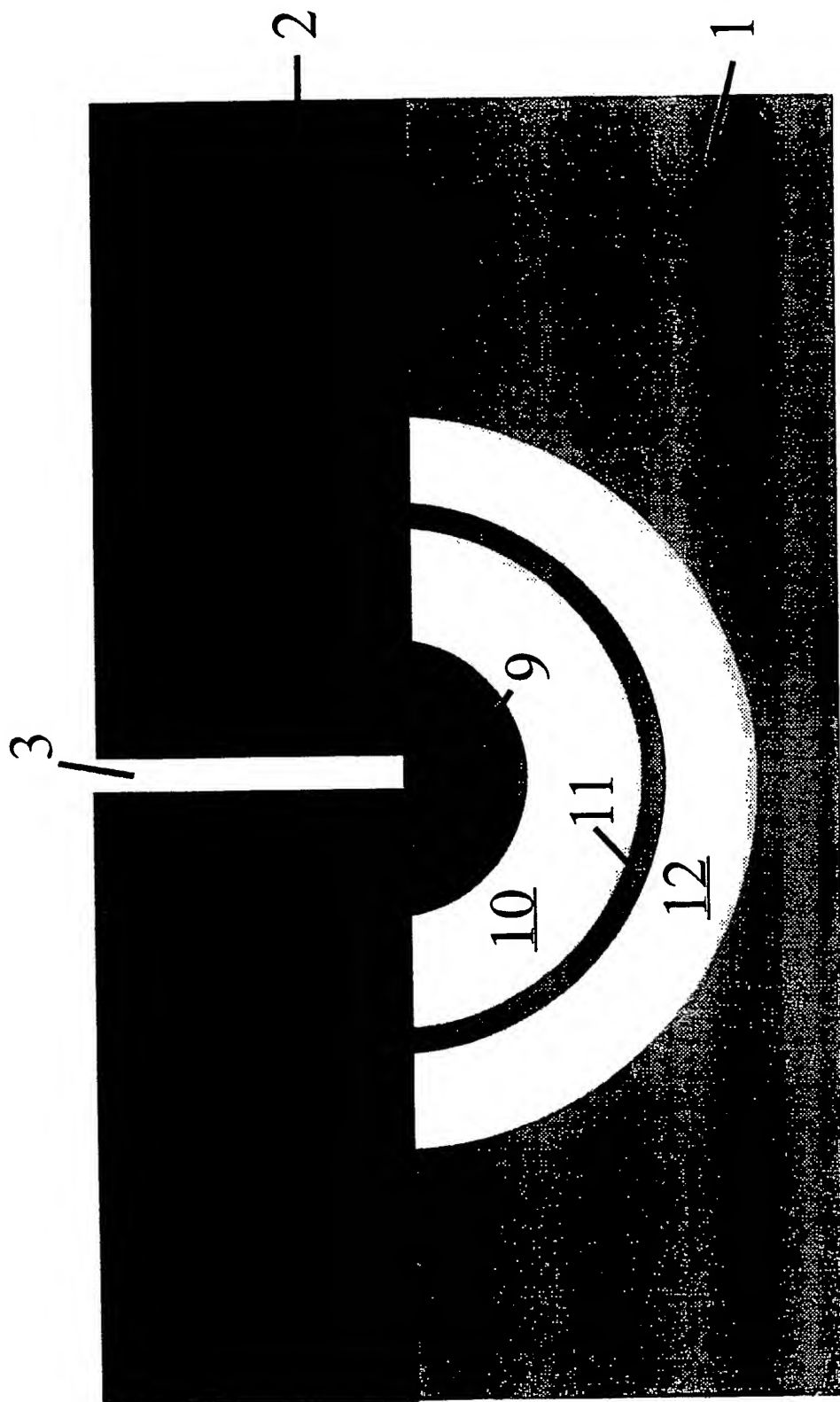


FIG. 2

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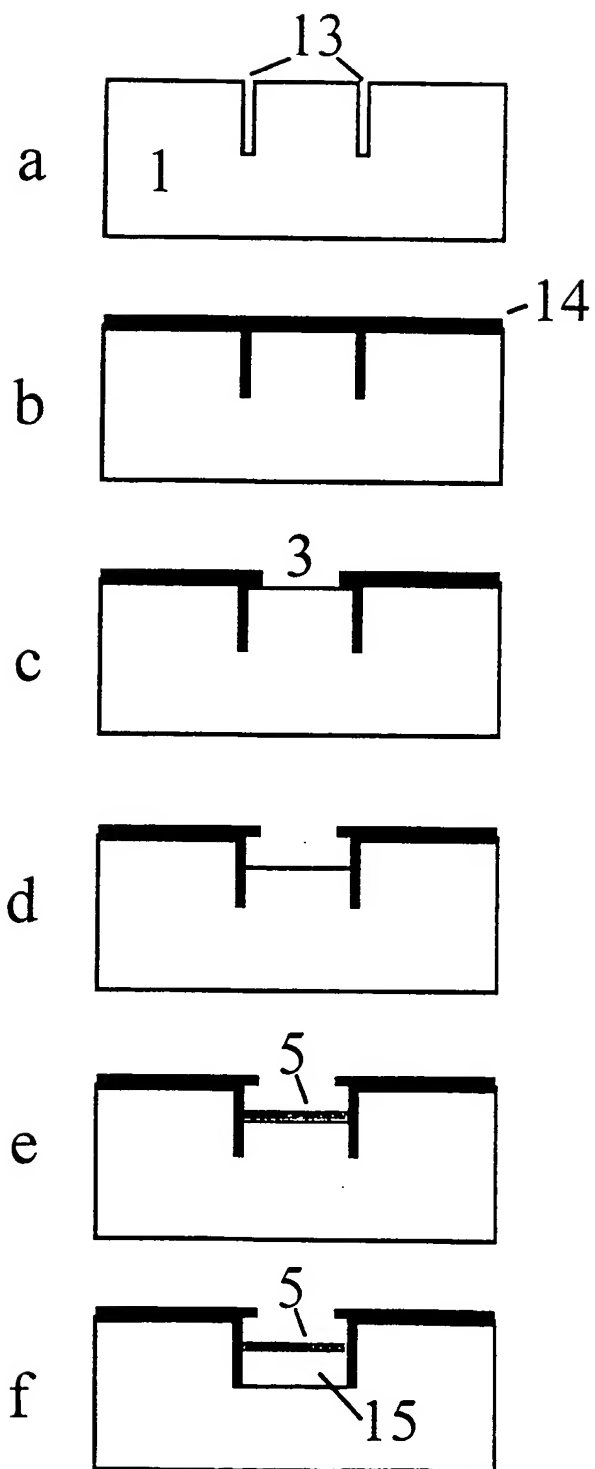


FIG. 3

INTERNATIONAL SEARCH REPORT

International Application No
PCT/NL 99/00111

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/3063 H01L21/306 B81C1/00 C25F3/14

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	BEHREN VON J ET AL: "PROPERTIES OF ULTRATHIN FILMS OF POROUS SILICON" JOURNAL OF VACUUM SCIENCE AND TECHNOLOGY: PART B, vol. 13, no. 3, May 1995, pages 1225-1229, XP000537393 see page 225, column 1, paragraph 2 - column 2	1
A	US 5 139 624 A (SEARSON PETER C ET AL) 18 August 1992 see column 4, line 11 - line 29 see column 5, line 45 - line 64 see column 7, line 13 - line 24; figures 2,8	1,2,6

☒ Further documents are listed in the continuation of box C.

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Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	TJERKSTRA R W ET AL: "Etching technology for chromatography microchannels" ELECTROCHIMICA ACTA, vol. 42, no. 20-22, 1997, page 3399-3406 XP004086710 see the whole document ---	1-8
P,A	DE 196 53 097 A (KERNFORSCHUNGSANLAGE JUELICH) 2 July 1998 -----	9

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

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Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 5139624	A	18-08-1992	NONE	
DE 19653097	A	02-07-1998	WO 9828781 A	02-07-1998

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